AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph in the specification beginning on page 8, line 2, with the following rewritten paragraph:

FIGS. 6A-6B are diagrams ~~FIG. 6 is a diagram~~ showing the configuration of a memory module in a second embodiment of the present invention.

Please replace the paragraph in the specification beginning on page 8, line 14, with the following rewritten paragraph:

FIGS. 11A-11B are diagrams ~~FIG. 11 is a diagram~~ showing the configuration of lines in the memory system of the present invention.

Please replace the paragraph in the specification beginning on page 8, line 19, with the following rewritten paragraph:

FIGS. 13A-13D are diagrams ~~FIG. 13 is a diagram~~ showing the configuration of another embodiment of a driver in the memory system of the present invention.

Please replace the paragraph in the specification beginning on page 8, line 25, with the following rewritten paragraph:

FIGS. 15A-15B are diagrams ~~FIG. 15 is a diagram~~ showing the configuration of a memory system in a fourth embodiment of the present invention.

Please replace the paragraph in the specification beginning on page 9, line 2, with the following rewritten paragraph:

FIGS. 16A-16B are diagrams ~~FIG. 16 is a diagram~~ showing the configuration of a memory module in a fourth embodiment of the present invention.

Please replace the paragraph in the specification beginning on page 9, line 13, with the following rewritten paragraph:

FIGS. 21A-21B are diagrams ~~FIG. 21 is a diagram~~ showing the configuration of a memory system in an eighth embodiment of the present invention.

Please replace the paragraph in the specification beginning on page 9, line 15, with the following rewritten paragraph:

FIGS. 22A-22B are diagrams ~~FIG. 22 is a diagram~~ showing the configuration of a memory system in a ninth embodiment of the present invention, FIG. 22(A) is a diagram showing the configuration of a DRAM package board, and FIG. 22(B) is a diagram showing the configuration of the memory system.

Please replace the paragraph in the specification beginning on page 10, line 6, with the following rewritten paragraph:

FIGS. 29A-29B are diagrams ~~FIG. 29 is a diagram~~ showing the configuration of a memory system in a thirteenth embodiment of the present invention.

Please replace the paragraph in the specification beginning on page 14, line 17 (paragraph [0043]), with the following rewritten paragraph:

FIGs. 1A and 1B is a diagram showing an example of the configuration of a memory module in accordance with a first embodiment of the present invention. FIG. 1A is a cross sectional view and FIG. 1B is a top view wherein one DQ bus line is shown. Referring to FIGs. 1A and [[1b]] 1B, a memory module in accordance with the present embodiment has a plurality of DRAMs 115, which share a bus line, on the front surface and the back surface of the module board. The bus line is extended on the front surface of the board from a first module terminal (DQ) 111 to a via hole 113 spaced from the first module terminal and is connected to one end of a first strip line 112 through the via hole 113. The signal terminal of a DRAM 115 mounted on the front surface of the board is connected to the first strip line 112 through an associated via hole. The first strip line is extended in one direction, and the other end corresponding to said one end is connected to the one end of a second strip line 112 on the back surface through a loop-back via hole 119. The second strip line 112 is extended in the direction opposite to the one direction, and the terminal of a DRAM 115 mounted on the back surface of the board is connected to the second strip line through an associated via hole. A termination resistor

provided near a voltage termination terminal (VTT) is mounted on the back surface of the board. The termination resistor 120 is connected to the other end of the looped back second strip line through a via hole.

Please replace the paragraph in the specification beginning on page 16, line 23 (paragraph [0050]), with the following rewritten paragraph:

FIG. 2 is a diagram showing an example of the configuration of a memory module in the first embodiment of the present invention. The memory module comprises 4-bit I/O DRAMs, command/address register (CA register) 121 that latches the command/address (Command Address) signal supplied from a chip set, not shown, to the DRAMs, terminating ~~register~~ resistor 120, DQ signal line, CA (Command Address) signal line, and clock signal line (CLK). The DQ signal line and the clock signal lines CLK and CLKB are connected from memory module terminals to the plurality of DRAM terminals in a stubless configuration and are terminated by the DRAM on-chip termination (build-in termination resistor) on the DRAM at the end. The CLK signal and CLKB signal are differential clock signals.

Please replace the paragraph in the specification beginning on page 33, line 25 (paragraph [0115]), with the following rewritten paragraph:

Next, the driver of the memory controller 2 according to the present invention and the generation of the reference voltage Vref will be described. As shown in FIG. 12, Vref (logic threshold voltage reference) may be generated using a memory with a built-in terminator 115 at

the end of the bus line in the memory module 1. In this embodiment, the memory controller 2 has a logic threshold voltage output circuit [[23]] 22.

Please replace the paragraph in the specification beginning on page 34, line 8 (paragraph [0116]), with the following rewritten paragraph:

Because the driver (output circuit) 21 is a push-pull circuit in accordance with this embodiment, the logic threshold voltage output circuit [[23]] 22, with a circuit configuration similar to that of the driver, may be implemented by a circuit in which the input terminal and the output terminal are shorted. The logic threshold voltage output circuit [[23]] 22 of the memory controller 2 is connected to the Vref line. The push-pull circuit, connected between the power supply and the ground (GND), comprises a PMOS transistor PM1 and an NMOS transistor NM1 which have gates connected in common to the input terminal, and drains connected in common to the output terminal (DQ terminal).